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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,641	07/29/2003	Shinsuke Anzai	299002056800	8273
25226	7590	09/22/2004	EXAMINER	
MORRISON & FOERSTER LLP 755 PAGE MILL RD PALO ALTO, CA 94304-1018			LE, THONG QUOC	
			ART UNIT	PAPER NUMBER
			2818	

DATE MAILED: 09/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/630,641	ANZAI ET AL.	
	Examiner	Art Unit	
	Thong Q. Le	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-7 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. ____. |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date ____. | 6) <input type="checkbox"/> Other: ____. |

DETAILED ACTION

1. Claims 1-7 are presented for examination.

Information Disclosure Statement

2. This office acknowledges receipt of the following items from the Applicant:
Information Disclosure Statement (IDS) filed on July 29, 2003.
3. Information disclosed and list on PTO 1449 was considered.

Priority

4. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

5. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application

by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

7. Claims 1-7 are rejected under 35 U.S.C. 102(e) as being anticipated by Kishimoto et al. (U.S. Patent No. 6,473,321).

Regarding claim 1 Kishimoto et al. disclose a semiconductor memory device (Figure 9) comprising:

a memory cell array (MAT-U, MAT-D) comprising a two-value memory region and a multi-value memory region (Column 14, lines 20-27), wherein the two-value memory region comprise a plurality of memory cells each storing 1-bit data and the multi-value memory region comprises a plurality of memory cells each storing 2 or more-bit data (Column 1, lines 40-57); and

a sense amplifier section (Figure 9, 36) common to data read of the two-value memory region and data read of the multi-value memory region, for reading data stored in a selected memory cell (Column 15, lines 19-26) by comparing a potential of the selected memory cell with a reference potential (Column 14, lines 8-19).

Regarding claims 2-7, Kishimoto et al. disclose a first switch section for switching the reference potential (Figure 9, 37), depending on whether data is read from

the two-value memory region or the multi-value memory region (Column 6, lines 51-67, Column 7, lines 1-22), and a conversion section (Figure 9, 20) for changing the number of bits in accordance with a result of a comparison performed by the sense amplifier section, and switching output data, depending on whether or not the data is read from the multi-value memory region or the two-value memory region (Column 15, lines 19-30), and wherein the conversion section has two or more output terminals (Figure 9, 20); and when data is read from the two-value memory region, the conversion section outputs the data through the output terminals, all bits of the data having the same value (Column 14, lines 20-24), and further comprising a redundant cell (Figure 9, 41) for replacing a defective memory cell in the memory cell array, if any; and a switch section (Figure 9, 371) for receiving data read from the redundant cell, and switching from the data read from the selected memory cell to the data read from the redundant cell when the selected memory cell is the defective memory cell (Column 15, lines 25-30), and further comprising: a write/delete control section (Figure 9, 33) for controlling data write or data delete for the two-value memory region and the multi-value memory region separately, wherein the sense amplifier section can perform data read for one of the two-value memory region and the multi-value memory region while the write/delete control section is performing data write or data delete for the other of the two-value memory region and the multi-value memory region (Column 15, lines 3-10), and wherein the write/delete control section can perform data write or data delete for one of the two-value memory region and the multi-value memory region while the sense

amplifier section is performing data read for the other of the two-value memory region and the multi-value memory region (Column 15, lines 3-30).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thong Q. Le
Primary Examiner
Art Unit 2818

THONG LE
PRIMARY EXAMINER